Notice of Allowability	Application No.	Applicant(s)	
	10/042,548	SHEREDY, JOSEPH	
	Examiner	Art Unit	
	Andre Pierre-Louis	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed on 11/16/2005*.

2. ☒ The allowed claim(s) is/are *1-32*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

1.0 The amendment filed on 11/16/2005 has been received and considered. Claims 1-32 are presented for examination.

Allowable Subject Matter

2.0 Claims 1-32 are allowed.

3.0 The following is an examiner's statement of reasons for allowance:

3.1 Regarding the independent claims 1,6,11, and 16, While Meyer teaches a method for testing a controller with random constraints, providing an IDE controller model having a primary and a secondary channel and a host interface; and Furukawa teaches a method and apparatus for testing a semiconductor having an A-D converting unit capable of generating high accurate test waveform of high speed including generating a first and a second waveform, a wave synthesizing unit, which may be an adder. None of these references cited taken alone or in combination disclose the testing of one SOC with another SOC having: a first SOC comprising a first hard disk controller and a first read channel; a second SOC comprising a second hard disk controller and a second read channel, as claimed by the applicant.

3.2 With regards to independent claim 21, Furukawa, as stated above, teaches a method and apparatus for testing a semiconductor having a first and a second waveform generating units, a comparator, a wave synthesizing unit which may be an adder; and Meyer teaches a method for testing a controller with random constraints, providing an IDE controller model having a primary and a secondary channel and a host interface. None of the these references taken alone or in

combination teaches the testing of a system on chip having: a first SOC and a second SOC, and the steps of: generating a timing signal; differentiating the timing signal; generating a write signal a write signal in synchronization with the differentiated timing signal by a second SOC; adding the write signal and timing signal; and inputting to the first SOC the timing signal and write signal component.

3.3 As per claim 24, Furukawa teaches a method and apparatus for testing a semiconductor having a first and a second waveform generating units, a comparator, a wave synthesizing unit which may be an adder, but does not disclose the testing of a first SOC with a second SOC and the connecting steps, as claims in the applicant's invention.

3.4 Turnquist (other reference cited) teaches a single semiconductor test system which behaves as multiple logic testers, each operating separately and asynchronously from the other. The semiconductor test system includes a host computer with means for generating test pattern to assigned pins of a semiconductor device under test.

3.5 None of the prior art of record, taken alone or in combination, disclose a method for testing a system on a chip having a first SOC comprising a first hard disk controller and a first read channel; a second SOC comprising a second hard disk controller and a second read channel, in combination with the remaining elements and features of the claimed invention. It is for these reasons that the applicant's invention defines over the prior art of record.

4.0 Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

5.0 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andre Pierre-Louis whose telephone number is 571-272-8636. The examiner can normally be reached on Mon-Fri, 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo P. Picard can be reached on 571-272-3749. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

January 12, 2006

APL

Paul L. Rodriguez 1/20/06

Primary Examiner
Art Unit 2125